EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	501	fixed with function with (accelerator coprocessor dsp slave)	US-PGPUB; USPAT	OR	ON	2008/08/19 16:41
L3	86	(fixed static) near3 function$4 with (accelerator coprocessor dsp slave) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:41
L4	76	(fixed static) near3 function$4 with (accelerator coprocessor dsp) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:42
L5	72	fixed near3 function$4 with (accelerator coprocessor dsp) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:43
L6	3	(hardcoded hardwired hard-wired hard-coded "hard wired" "hard coded") with fixed near3 function$4 with (accelerator coprocessor dsp) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:44
L7	10	(hardcoded hardwired hard-wired hard-coded "hard wired" "hard coded") with fixed with (accelerator coprocessor dsp) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:45
L8	913	345/501.ccls.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:51
L9	328	345/503.ccls.	US-PGPUB; USPAT	OR	ON	2008/08/19 16:51
L10	173	345/503.ccls. and (register memory buffer queue fifo) with (input source data value operand) same result	US-PGPUB; USPAT	OR	ON	2008/08/19 16:53
L11	60	345/503.ccls. and (register memory buffer queue fifo) with (input source data value operand) same result same transfer$4	US-PGPUB; USPAT	OR	ON	2008/08/19 16:53

L12	10	345/503.ccls. and ((register memory buffer queue fifo) with (input source data value operand) same result same transfer$4) and (accelerator coprocessor dsp slave) with (fixed static hardcoded hardwired hard-wired hard-coded "hard wired" "hard coded")	US-PGPUB; USPAT	OR	ON	2008/08/19 17:03
S1	86	pipeline near2 accelerator	US-PGPUB; USPAT	OR	ON	2006/06/19 11:11
S2	884	pipeline with accelerat $3	US-PGPUB; USPAT	OR	ON	2006/06/19 11:11
S3	220	pipeline near2 accelerat $3	US-PGPUB; USPAT	OR	ON	2006/10/03 13:45
S4	26	pipeline near2 accelerat $3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/19 11:17
S5	0	accelerat$3 with load$3 with process$3 with external and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/19 11:17
S6	44	accelerat$3 with load$3 with process$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 08:19
S7	3	("5583964" "4956771" "5892962").pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:21
S8	10	mccarthy-paul.in.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:52
S9	1	"5619430".pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:53
S10	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:54
S11	8	"raw data" with (coprocessor co-processor) same (buffer queue FIFO)	US-PGPUB; USPAT	OR	ON	2006/06/20 10:56
S12	31	"raw data" with (coprocessor co-processor)	US-PGPUB; USPAT	OR	ON	2006/06/20 14:51
S13	171	"raw data" with (slave PE DSP)	US-PGPUB; USPAT	OR	ON	2006/06/20 14:51
S14	9	"raw data" with (slave PE DSP) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 14:54

S15	12	"processed data" with (coprocessor co-processor) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 14:54
S16	1	(US-6624819-$).did.	USPAT	OR	ON	2006/06/21 08:41
S17	1	S16 and "160" with ("204" "206")	US-PGPUB; USPAT	OR	ON	2006/06/21 10:16
S18	165	output near2 queue with (address$2 pointer) near3 memory	US-PGPUB; USPAT	OR	ON	2006/06/21 10:22
S19	77	output near2 queue near5 (address$2 pointer) near2 memory	US-PGPUB; USPAT	OR	ON	2006/06/21 10:17
S20	19	output near2 queue near5 (address$2 pointer) near2 memory and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2006/06/21 10:17
S21	34	output near2 queue with (address$2 pointer) near3 memory and g06f $.ipc. not S20	US-PGPUB; USPAT	OR	ON	2006/06/21 11:06
S22	482	address near2 queue with (address$2 pointer) near3 memory and g06f $.ipc. not S20	US-PGPUB; USPAT	OR	ON	2006/06/21 10:22
S23	2	opcode near3 coprocessor with (send $3 transfer$4 transmit $4) with instruction	US-PGPUB; USPAT	OR	ON	2006/06/22 08:39
S30	1480	receiv$3 near3 data same tempora$4 near3 stor$3 same process$3 near3 data same (transmi$5 send$3 pass $3) near4 data	US-PGPUB; USPAT	OR	ON	2006/09/27 14:42
S31	538	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process $3 near3 data) same ((transmi$5 send$3 pass $3) near3 data with process$3)	US-PGPUB; USPAT	OR	ON	2006/09/27 14:43
S32	5	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process $3 near3 data) same ((transmi$5 send$3 pass $3) near3 data with process$3) same (pipeline accelerat$3)	US-PGPUB; USPAT	OR	ON	2006/09/27 14:45

S33	1	((data near3 tempora$4 near3 stor$3) with (prior before) near3 process $3) same ((transmi$5 send$3 pass$3) same (pipeline accelerat$3))	US-PGPUB; USPAT	OR	ON	2006/09/28 08:37
S34	84	((processor pipeline) with first near3 integrated adj circuit) and (memory DRAM) with (separate second) near3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2006/09/28 08:41
S35	177	((processor pipeline) with memory with separate near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:42
S36	38	((processor pipeline) with memory with separate near3 integrated adj circuit) same advantag$4	US-PGPUB; USPAT	OR	ON	2006/09/28 08:46
S37	3	((processor pipeline) with memory with separate near3 integrated adj circuit) same (faster speed failure)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S38	0	((processor pipeline) with memory with separate near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S39	0	((processor pipeline) with memory with distinct near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S40	73	((processor pipeline) with memory with integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:51
S41	237	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/10/03 13:48

S42	41	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit) same (benefi$5 advantag $6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:54
S43	417	((processor pipeline) with memory with integrated adj circuit) same (benefi$5 advantag $6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:54
S44	73	((processor pipeline) with memory with single near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:56
S45	1	((processor pipeline) with memory with (two multiple plurality) near3 integrated adj circuit) same (benefi$5 advantag $6)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:25
S46	18	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (memory near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S47	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (DRAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S48	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (RAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S49	130	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:28

S50	3	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:29
S51	15	((processor pipeline) with (DRAM RAM memory) with separate near2 chip) same (benefi $5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:39
S52	85	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) same (benefi $5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:43
S53	21	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) with (benefi $5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:41
S54	64	S52 not S53	US-PGPUB; USPAT	OR	ON	2006/09/28 10:12
S55	49	(memory DRAM RAM) with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:41
S56	0	("register file") with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:42
S57	86	("register file") with ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:43
S58	48	("register file") near3 ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:04
S59	199	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:07

S60	22	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/28 11:59
S61	27742	buffer with ("integrated circuit" chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:59
S62	6	buffer near3 separate near3 ("integrated circuit" chip) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2006/09/29 11:20
S63	34	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2006/09/28 12:01
S64	44	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline CPU)	US-PGPUB; USPAT	OR	ON	2006/09/29 08:11
S65	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2006/09/29 08:11
S66	7	("2" two) near2 stage near3 (multiplier multiply multiplication) with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:23
S67	38	multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:28
S68	0	coprocessor same multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:28
S69	47	coprocessor with multipl $7 adj accumulat$3	US-PGPUB; USPAT	OR	ON	2006/09/29 13:10
S70	276	pointer with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2006/09/29 13:10
S71	38	pointer with next with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2006/09/29 13:12
S72	7	read adj pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:14
S73	20	pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:16

S74	3	pointer with buffer with input with (execution functional) near2 unit and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:18
S75	43	pointer with buffer with input with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:19
S76	151	pointer with buffer with (operand data) with read $3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:19
S77	29	pointer with buffer with operand with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:22
S78	125	read near3 pointer near3 buffer and "712"/ $.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:23
S79	112	read near2 pointer near3 buffer and "712"/ $.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:24
S80	24	queue near3 pointer near3 buffer and "712"/ $.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:34
S81	13	queue near2 pointer near3 buffer and "712"/ $.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:35
S82	25	(queue fifo) near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:38
S83	5	stor$3 near5 buffer near2 pointer near5 queue and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 15:43
S84	14	processor with coprocessor with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:26
S85	109	"front end" with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S86	61	"front end" near3 separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S87	0	"front end" near3 separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S88	4	"front end" with separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 09:34

S89	3	coprocessor with execut $3 with (division divide) near3 (operation instruction) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 12:36
S90	319	712/34.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:02
S91	250	712/35.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:03
S92	405	712/200.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:04
S93	595	712/225.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:08
S94	1	"6282627".pn.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:08
S95	67	pipeline near2 accelerat $3	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 13:48
S96	3	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 13:49
S97	4	coprocessor with message with header	US-PGPUB; USPAT	OR	ON	2007/05/04 10:46
S98	22	coprocessor with (packet instruction) with header	US-PGPUB; USPAT	OR	ON	2007/05/04 10:47
S99	12	("4991133" | "5619497" | "5991299" | "6317837" | "6408001" | "6434620" | "6496704" | "6498793" | "6661794" | "6687757" | "6757725" | "6789147").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/04 11:13
S100	10	S99 and header	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/04 11:13
S101	7	S99 and header same $2processor	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/04 11:13
S102	155	tag with destination with register with (result data)	US-PGPUB; USPAT	OR	ON	2007/05/04 14:18
S103	0	tag with destination with register with (result data) with coprocessor	US-PGPUB; USPAT	OR	ON	2007/05/04 14:18
S105	67	huisman.xa.	US-PGPUB; USPAT	OR	ON	2007/12/12 16:11

S106	22	nakajima.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/12 18:00
S107	9	nakagoshi.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 10:57
S108	0	coprocessor with header with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/13 10:57
S109	3	coprocessor with (message packet) with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/13 11:01
S110	6480	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send $3)	US-PGPUB; USPAT	OR	ON	2007/12/13 11:02
S111	48	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send $3) same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:10
S112	0	first near2 PE with second near2 PE with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:10
S113	1544	first near2 PE ("processing element") with second near2 (PE "processing element") same header same result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:26
S114	1544	first near2 PE ("processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:27
S115	0	first near2 (PE "processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:27

S117	0	(PE "processing element") with message with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:28
S118	0	(PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:28
S119	28	(PE "processing element") with message with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 13:17
S120	10	(PE "processing element") with among with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 13:18
S121	0	(PE "processing element") with amongst with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 13:18
S122	1	(US-4985832-$).did.	USPAT	OR	ON	2007/12/13 13:48
S123	1	S122 and memory with message	USPAT	OR	ON	2007/12/13 18:16
S124	706	latch near2 memory near2 address	USPAT	OR	ON	2007/12/13 18:17
S125	474	latch near2 memory near2 address and (advantage benefit)	USPAT	OR	ON	2007/12/13 18:17
S126	1	latch near2 memory near2 address with (advantage benefit)	USPAT	OR	ON	2007/12/13 18:17
S127	405	latch near2 (memory adj address)	USPAT	OR	ON	2007/12/13 18:20
S128	262	latch with (provid$3 allow$3) with (synchronous synchronized)	USPAT	OR	ON	2007/12/13 18:21
S129	1	latch with (provid$3 allow$3) with (synchronous synchronized) same (advantage benefit)	USPAT	OR	ON	2007/12/13 18:21
S130	49	latch with (provid$3 allow$3) with (synchronous synchronized) and g06f$.ipc.	USPAT	OR	ON	2007/12/13 18:22
S131	98	pipeline near2 accelerator	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38

S132	1038	pipeline with accelerat $3	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S133	261	pipeline near2 accelerat $3	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S134	47	pipeline near2 accelerat $3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S135	2	accelerat$3 with load$3 with process$3 with external and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S136	71	accelerat$3 with load$3 with process$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S137	3	("5583964" "4956771" "5892962").pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S138	10	mccarthy-paul.in.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S139	1	"5619430".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S140	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S141	8	"raw data" with (coprocessor co-processor) same (buffer queue FIFO)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S142	42	"raw data" with (coprocessor co-processor)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S143	208	"raw data" with (slave PE DSP)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S144	9	"raw data" with (slave PE DSP) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S145	19	"processed data" with (coprocessor co-processor) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S146	1	(US-6624819-$).did.	USPAT	OR	ON	2007/12/14 11:38
S147	1	S146 and "160" with ("204" "206")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S148	193	output near2 queue with (address$2 pointer) near3 memory	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S149	90	output near2 queue near5 (address$2 pointer) near2 memory	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38

S150	21	output near2 queue near5 (address$2 pointer) near2 memory and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S151	38	output near2 queue with (address$2 pointer) near3 memory and g06f $.ipc. not S150	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S152	551	address near2 queue with (address$2 pointer) near3 memory and g06f $.ipc. not S150	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S153	2	opcode near3 coprocessor with (send $3 transfer$4 transmit $4) with instruction	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S154	1791	receiv$3 near3 data same tempora$4 near3 stor$3 same process$3 near3 data same (transmi$5 send$3 pass $3) near4 data	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S155	22	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process $3 near3 data) same ((transmi$5 send$3 pass $3) near3 data with process$3) same (pipeline accelerat$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S156	1	((data near3 tempora$4 near3 stor$3) with (prior before) near3 process $3) same ((transmi$5 send$3 pass$3) same (pipeline accelerat$3))	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S157	658	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process $3 near3 data) same ((transmi$5 send$3 pass $3) near3 data with process$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S158	100	("register file") with ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S159	98	((processor pipeline) with memory with integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38

S160	108	((processor pipeline) with first near3 integrated adj circuit) and (memory DRAM) with (separate second) near3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S161	27	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) with (benefi $5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S162	0	((processor pipeline) with memory with separate near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S163	48	("register file") near3 ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
S164	59	(memory DRAM RAM) with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S165	49	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit) same (benefi$5 advantag $6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S166	3	((processor pipeline) with memory with separate near3 integrated adj circuit) same (faster speed failure)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S167	44	((processor pipeline) with memory with separate near3 integrated adj circuit) same advantag$4	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S168	219	((processor pipeline) with memory with separate near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S169	0	((processor pipeline) with memory with distinct near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S170	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (RAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S171	3	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S172	522	((processor pipeline) with memory with integrated adj circuit) same (benefi$5 advantag $6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S173	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (DRAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S174	298	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S175	163	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S176	93	((processor pipeline) with memory with single near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S177	20	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (memory near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S178	1	((processor pipeline) with memory with (two multiple plurality) near3 integrated adj circuit) same (benefi$5 advantag $6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S179	24	((processor pipeline) with (DRAM RAM memory) with separate near2 chip) same (benefi $5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S180	98	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) same (benefi $5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S181	0	("register file") with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S182	71	S180 not S161	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S183	37	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S184	251	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S185	32010	buffer with ("integrated circuit" chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S186	30	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S187	48	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline CPU)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S188	6	buffer near3 separate near3 ("integrated circuit" chip) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S189	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S190	7	("2" two) near2 stage near3 (multiplier multiply multiplication) with latch	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S191	54	coprocessor with multipl $7 adj accumulat$3	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S192	42	multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S193	0	coprocessor same multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S194	26	pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S195	32	pointer with buffer with operand with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S196	313	pointer with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S197	8	pointer with buffer with input with (execution functional) near2 unit and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S198	44	pointer with next with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S199	54	pointer with buffer with input with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S200	196	pointer with buffer with (operand data) with read $3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S201	10	read adj pointer with "input buffer" and "712"/ $.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S202	142	read near2 pointer near3 buffer and "712"/ $.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S203	155	read near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S204	31	(queue fifo) near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S205	18	queue near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S206	7	stor$3 near5 buffer near2 pointer near5 queue and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S207	31	queue near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S208	17	processor with coprocessor with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S209	141	"front end" with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S210	4	"front end" with separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S211	0	"front end" near3 separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S212	78	"front end" near3 separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S213	4	coprocessor with execut $3 with (division divide) near3 (operation instruction) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S214	370	712/34.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S215	270	712/35.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S216	437	712/200.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S217	683	712/225.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S218	1	"6282627".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S219	3	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/14 11:39
S220	71	pipeline near2 accelerat $3	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/14 11:39
S221	12	("4991133" | "5619497" | "5991299" | "6317837" | "6408001" | "6434620" | "6496704" | "6498793" | "6661794" | "6687757" | "6757725" | "6789147").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:39
S222	7	S221 and header same $2processor	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:39
S223	5	coprocessor with message with header	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S224	157	tag with destination with register with (result data)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S225	10	S221 and header	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:39
S226	24	coprocessor with (packet instruction) with header	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S227	0	tag with destination with register with (result data) with coprocessor	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S228	67	huisman.xa.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S229	22	nakajima.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S230	9	nakagoshi.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S231	0	coprocessor with header with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S232	3	coprocessor with (message packet) with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S233	0	(PE "processing element") with message with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S234	6480	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send $3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S235	1544	first near2 PE ("processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S236	0	first near2 (PE "processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S237	1544	first near2 PE ("processing element") with second near2 (PE "processing element") same header same result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S238	0	first near2 PE with second near2 PE with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S239	28	(PE "processing element") with message with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S240	0	(PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S241	48	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send $3) same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S242	10	(PE "processing element") with among with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

S243	1	(US-4985832-$).did.	USPAT	OR	ON	2007/12/14 11:39
S244	1	S243 and memory with message	USPAT	OR	ON	2007/12/14 11:39
S245	0	(PE "processing element") with amongst with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
S246	706	latch near2 memory near2 address	USPAT	OR	ON	2007/12/14 11:39
S247	474	latch near2 memory near2 address and (advantage benefit)	USPAT	OR	ON	2007/12/14 11:39
S248	1	latch near2 memory near2 address with (advantage benefit)	USPAT	OR	ON	2007/12/14 11:39
S249	49	latch with (provid$3 allow$3) with (synchronous synchronized) and g06f$.ipc.	USPAT	OR	ON	2007/12/14 11:39
S250	1	latch with (provid$3 allow$3) with (synchronous synchronized) same (advantage benefit)	USPAT	OR	ON	2007/12/14 11:39
S251	405	latch near2 (memory adj address)	USPAT	OR	ON	2007/12/14 11:39
S252	262	latch with (provid$3 allow$3) with (synchronous synchronized)	USPAT	OR	ON	2007/12/14 11:39
S253	42	(2001/0014937 2001/0025338 2002/0087829 2003/0009651 2003/0061409 2003/0177223 2004/0019771 2004/0019883 2004/0045015 2004/0061147 2004/0064198 2004/0130927 2004/0133763 2004/0136241 2004/0153752 2004/0170070 2005/0104743 2006/0123282 2006/0236018 2007/0055907	US-PGPUB; USPAT	OR	ON	2008/08/08 13:26

		"4703475" "4873626" "5283883" "5317752" "5623418" "5640107" "5655069" "5784636" "5801958" "5867399" "5910897" "5916307" "5931959" "5933356" "6018793" "6023742" "6049222" "6096091" "6108693" "6112288" "6205516" "6216191" "6216252" "6247118" "6253276" "6282627" "6308311" "6324678" "6326806" "6470482" "6625749" "6662285" "6684314" "6769072" "6785842" "6829697" "6839873" "6982976" "7117390" "7134047" "7137020" "7228520").pn.				
S254	20	("20010014937" "20010025338" "20020087829" "20030009651" "20030061409" "20030177223" "20040019771" "20040019883" "20040045015" "20040061147" "20040064198" "20040130927" "20040133763" "20040136241" "20040153752" "20040170070" "20050104743" "20060123282" "20060236018" "20070055907").pn.	US-PGPUB; USPAT	OR	ON	2008/08/08 13:27
S255	16	fpga near3 (pipeline accelerator) and (data message packet) same header same destination same (fpga pipeline accelerator)	US-PGPUB; USPAT	OR	ON	2008/08/18 14:30
S256	1	"6282627".pn.	US-PGPUB; USPAT	OR	ON	2008/08/18 14:37
S257	1	"6982976".pn.	US-PGPUB; USPAT	OR	ON	2008/08/18 14:43

S258	298	(data message packet) same header same destination same (fpga pipeline accelerator)	US-PGPUB; USPAT	OR	ON	2008/08/18 14:46
S259	116	(data message packet) same header same destination same (fpga accelerator)	US-PGPUB; USPAT	OR	ON	2008/08/18 14:47
S260	82	(data message packet) same header same destination same fpga	US-PGPUB; USPAT	OR	ON	2008/08/18 14:47
S261	15	(data message packet) same header same destination same fpga and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/18 14:47
S262	0	coprocessor with fpga same hardware same without near2 (software instruction)	US-PGPUB; USPAT	OR	ON	2008/08/18 15:38
S263	38	coprocessor with implement$5 with fpga	US-PGPUB; USPAT	OR	ON	2008/08/18 15:39
S264	103	fpga same without near2 (software instruction)	US-PGPUB; USPAT	OR	ON	2008/08/18 15:40
S265	67	fpga same hardware same without near2 (software instruction)	US-PGPUB; USPAT	OR	ON	2008/08/18 15:40
S266	42	fpga same hardware same without adj2 (software instruction)	US-PGPUB; USPAT	OR	ON	2008/08/18 15:41
S267	0	fpga same hardware same without adj2 instruction	US-PGPUB; USPAT	OR	ON	2008/08/18 15:41
S268	0	fpga same without adj2 instruction	US-PGPUB; USPAT	OR	ON	2008/08/18 15:41
S269	0	"coprocessor ID" same CID	US-PGPUB; USPAT	OR	ON	2008/08/18 15:48
S270	17	(coprocessor and interface).ti.	US-PGPUB; USPAT	OR	ON	2008/08/18 15:48
S271	409	712/34.ccls.	US-PGPUB; USPAT	OR	ON	2008/08/18 15:49
S272	80	712/34.ccls. and coprocessor.ti.	US-PGPUB; USPAT	OR	ON	2008/08/18 15:50
S273	22	coprocessor.ti. and coprocessor with ID	US-PGPUB; USPAT	OR	ON	2008/08/18 15:50
S276	5671	any with logic with implement$5 with fpga	US-PGPUB; USPAT	OR	ON	2008/08/18 16:23
S277	23	(any all) adj logic with implement$5 with fpga	US-PGPUB; USPAT	OR	ON	2008/08/18 16:23

S278	18	(any all) adj logic with implement$5 with field adj programmable adj gate adj array	US-PGPUB; USPAT	OR	ON	2008/08/18 16:25
S279	5	(pipeline accelerator) with burn$2 with (die chip substrate)	US-PGPUB; USPAT	OR	ON	2008/08/18 16:26
S280	141	logic with burn$2 with (die chip substrate)	US-PGPUB; USPAT	OR	ON	2008/08/18 16:27
S281	25	logic with burn$2 with (die chip substrate) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/18 16:27
S282	0	coprocessor with burn$2 with (die chip substrate) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/18 16:28
S283	123	process$3 near2 data with without near3 execut$3 near3 instruction	US-PGPUB; USPAT	OR	ON	2008/08/18 16:50
S284	41	process$3 near2 data with without adj3 execut $3 adj3 instruction	US-PGPUB; USPAT	OR	ON	2008/08/18 16:50
S285	19	process$3 near2 data with without adj execut $3 adj3 instruction	US-PGPUB; USPAT	OR	ON	2008/08/18 16:50
S286	21	(processor CPU master) with offload$3 with fpga	US-PGPUB; USPAT	OR	ON	2008/08/18 16:57
S287	3	(processor CPU master) with offload$3 with (pld pla)	US-PGPUB; USPAT	OR	ON	2008/08/18 16:59
S288	9	(processor CPU master) with (coupl$3 connect $3) with (multiple plurality) near2 fpga	US-PGPUB; USPAT	OR	ON	2008/08/19 09:20
S289	22	(processor CPU master) with fpga adj array	US-PGPUB; USPAT	OR	ON	2008/08/19 09:23
S290	2	(processor CPU master) with (coupl$3 connect $3) with (multiple plurality) near2 fpga	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/19 09:24
S291	117	(processor CPU master) with (connect$3 coupl $3) with $2configur$5 with logic with block	US-PGPUB; USPAT	OR	ON	2008/08/19 09:27
S292	26	(processor CPU master) with (connect$3 coupl $3) with (multiple plurality array) with $2configur$5 with logic with block	US-PGPUB; USPAT	OR	ON	2008/08/19 09:27

S293	3	("5757207" | "5768598" | "5883526").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/19 09:40
S294	5	("5864554" | "5943481" | "5950012" | "6012099" | "6070003").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/08/19 09:53
S295	3	(processor CPU master) with (connect$3 coupl $3) with (multiple plurality array) with CLB	US-PGPUB; USPAT	OR	ON	2008/08/19 09:55
S296	471	(CLB ($2configur$5 adj logic adj block)) with memory with data	US-PGPUB; USPAT	OR	ON	2008/08/19 09:57
S297	19	(CPU master processor) with (CLB ($2configur$5 adj logic adj block)) with (memory RAM buffer queue fifo) with (data operand)	US-PGPUB; USPAT	OR	ON	2008/08/19 09:58
S298	102	(CPU master processor) with accelerator and accelerator with (MAC (multipl$7 with accumulat$3))	US-PGPUB; USPAT	OR	ON	2008/08/19 11:59
S299	37	(CPU master processor) with accelerator and (accelerator with (MAC (multipl$7 with accumulat$3)) same (buffer memory queue register fifo) with (source operand data input value))	US-PGPUB; USPAT	OR	ON	2008/08/19 12:01
S300	18	(CPU master processor) with accelerator and (accelerator with (MAC (multipl$7 with accumulat$3)) same (buffer memory queue register fifo) with (source operand data input value)) and header	US-PGPUB; USPAT	OR	ON	2008/08/19 12:12
S301	727	"configurable logic block" and ("configurable logic block" CLB) with (buffer memory queue register fifo) with (source operand data input value)	US-PGPUB; USPAT	OR	ON	2008/08/19 12:18

S302	57	"configurable logic block" and ("configurable logic block" CLB) with (buffer memory queue register fifo) with (source operand data input value) and header	US-PGPUB; USPAT	OR	ON	2008/08/19 12:18
S303	1	"configurable logic block" and ("configurable logic block" CLB) with (buffer memory queue register fifo) with (source operand data input value) and header and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2008/08/19 12:19
S304	564	broadcast$3 with (instruction message) with (advantag$4 benefi $4)	US-PGPUB; USPAT	OR	ON	2008/08/19 13:04
S305	147	broadcast$3 with (instruction message) with (advantag$4 benefi $4) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 13:04
S306	118	broadcast$3 with (instruction message) with (advantag$4 benefi $4) and (ID header identification) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 13:05
S307	16	broadcast$3 with (instruction message) with (advantag$4 benefi $4) same (ID header identification) and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2008/08/19 13:05

8/19/08 6:13:08 PM
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